Putting Blind Vias in SMD Pads: *"Where They Belong"*

by

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ABSTRACT
Electronic manufacturers continue to design increased product functionality and performance. Pressures to reduce the size of a product, drive product costs down and shorten product development cycles continue to increase component interconnect densities at the circuit board level. The options are: increase the number of layers for routing traces, reduce space and trace widths, reduce via and pad sizes, or use blind vias within surface mount pads. Realistically, all the above options should be considered. The primary bottleneck is the via pad on the circuit board design blocking routing channels. This paper will discuss the options and show the most effective consideration is the via-in-pad interconnection.

Key words: Laser-drilled, Via-in-Pad, Blind Via.

INTRODUCTION
Ball Grid Array (BGA) and micro-BGA interconnect are challenging and demand increased circuit density. This increased component density demand is also fueled by the demand of other components with increased Input/Output (I/O) readily revealing the shortcomings in circuit board interconnect technology. No longer can fine pitch line widths and small mechanically drilled holes economically accommodate the increased requirements for circuit density. The lack of surface area to drill through vias is called Via Starvation.

Microvias were on the national Technology Roadmap wish list in 1993. Today, more than half dozen companies worldwide are offer solutions to providing interconnecting vias in the order of 50 micron diameter. These numbers were unheard of several years ago and provide an incentive to develop new algorithms for computer-aided design (CAD) routing tools, as well as developing new manufacturing processes. [1]

The use of vias in interconnecting surface mount devices (SMD's) can be loosely divided into two categories. First, those vias necessary to move between routing layers to enable an interconnect to be established from one component pin to another. Secondly, the " vias required at most SMD component pins that serve to connect between a surface layer where the SMD pin exists, and internal routing layers where most interconnections on dense SMD boards are forced.

It is this second group, the "fanout" vias, placed between and around fine pitch SMD pads that play the major role in limiting board density, increasing layer count, and because they use up potential via sites for the first type of via described, aid in creating a "via starvation" or gridlock condition.

Placing "fanout" vias within the SMD component pad represents a giant leap in SMD connectability without the need for ultra fine line and very small mechanically drilled holes and their associated costs.

One emerging solution for the *"Interconnection Gap" or "Via Starvation"* is blind via technology. To further expand and define the best blind via solution one is lead to Via-in-Pad. A Via-in-Pad interconnection provides the most effective Z-Axis interconnection when viewed from the circuit board design perspective.

There are several methods for fabricating blind vias:

- Mechanically drilled- limited depth
- Mechanically drilled- sequential lamination
- Laser drilled with or without copper mask
- Sequential build up - Photo Via defined
- Sequential buildup- Plasma Etched

Mechanically drilled blind vias have been used for over three decades and have proven over time to be too expensive. All of the blind via technologies listed above can readily be designed and fabricated to accommodate Via-in-Pad interconnections, however one of these blind via technologies shines above the rest when introduced into the conventional fabrication process - laser drilled Via-in-Pad technology.

The two blind via technologies that fall into the category of sequential buildup technologies [2,3], are Photo Via and Plasma Etched. These two technologies are finding early acceptance as blind via fabrication processes, but significant increases in fabrication costs occur when multi-depth (layers 1-2-3) interconnections are designed into the circuit board.

DESIGN CONSIDERATIONS

From the designers viewpoint, the problem is one of interconnect availability and is fueled by increasingly complex electrical circuitry and the reduction in product size. It has reached a critical point. Board densities formerly reserved for our nightmares are now waiting for us in the morning. High pin count devices such as BGA's present unprecedented design challenges. Up to now, the only available methods of dealing with the board density problem have been:

- Increase board layers,
- Decrease line and space geometry's,
- Reduce via pad and drill sizes,
- Use partial or blind vias.

Adding Board Layers

This obvious solution does increase potential routing channels, however, at a price. Each layer pair added, while increasing board cost by fifteen to twenty percent, requires more vias to utilize these added routing channels. On a dense SMD board all or nearly all potential via sites can be used up resulting in a "via starvation" or gridlock condition as shown in the drawing below (Fig. 1).

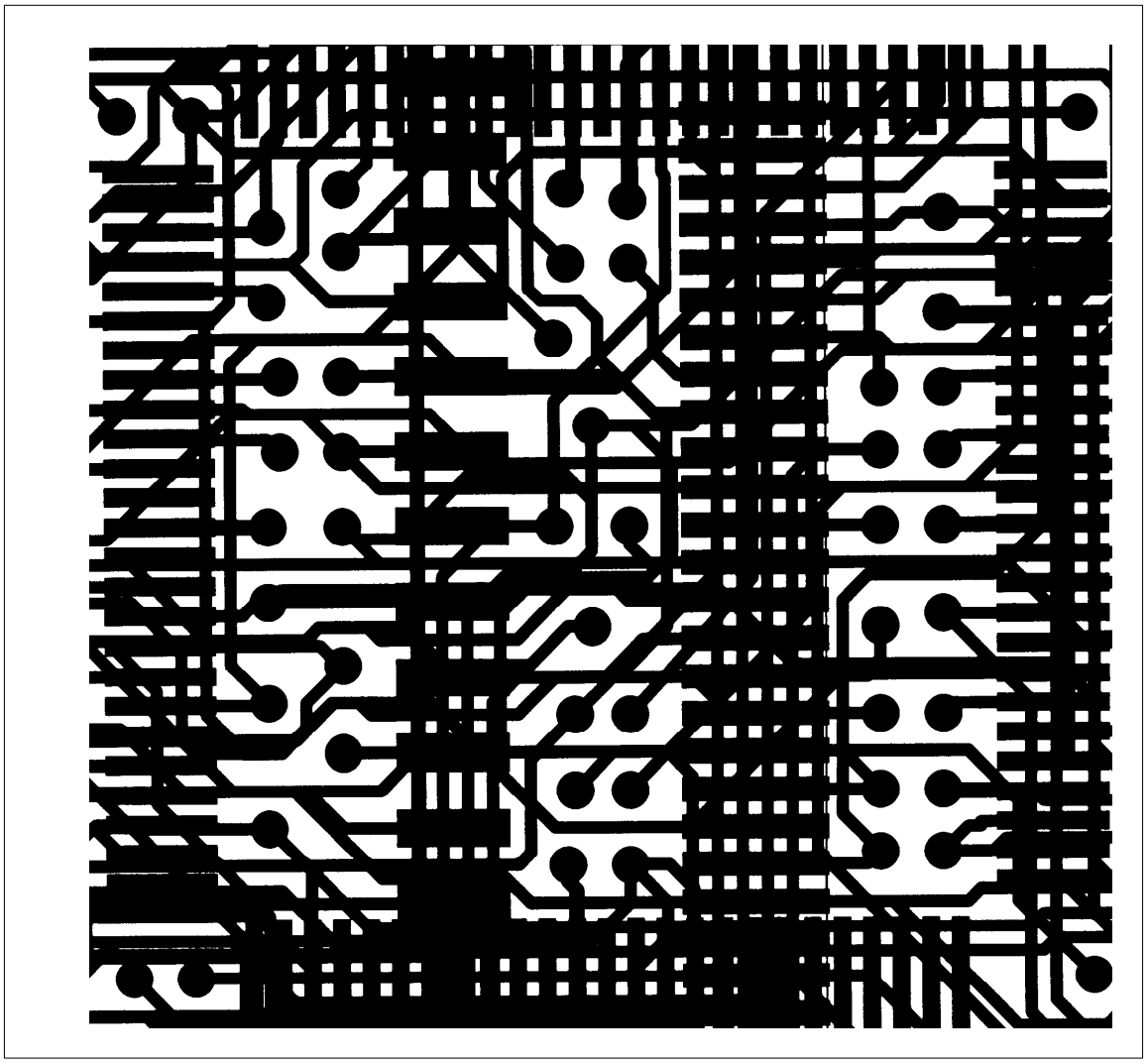


Fig. 1
"Via Starvation" - 4 of 6 Signal Layers Shown

Reduce Trace and Space Sizes

Many board manufacturers routinely produce trace & space widths of .0.13mm and 0.15mm While this is impressive, and aids board layout, the cost associated with the special handling and clean environment required to reduce trace and space beyond this point is prohibitive. Furthermore, this can only be a partial solution if not coupled with a substantial reduction in via size.

Reduce Via Size

Reducing via and pad sizes does not represent much potential for I increasing overall routability. Reducing via hole sizes beyond the practical low end limitation of 0.25mm/0.30mm on a 0.51mm/0.61mm pad would skyrocket costs as well as introducing other practical problems such as high aspect ratio plating and long term reliability.

Partial or Blind Vias

The use of partial or blind vias represents the greatest opportunity for improving routability of any of the options currently available. Of the blind via types discussed above, laser drilled blind vias are the superior solution for two reasons. First, laser vias are small! At 0.10mm/0.15mm on a 0.20mm/0.25mm pad they offer a savings in routing channels that mechanically drilled vias can approach. The second big reason is location. Small enough to fit even in the narrowest of fine pitch SMD component pads, laser vias completely eliminate the need for the sprawling array of "fan-out" vias necessary to connect SMD pads to inner trace routing layers as shown in Fig. 2.

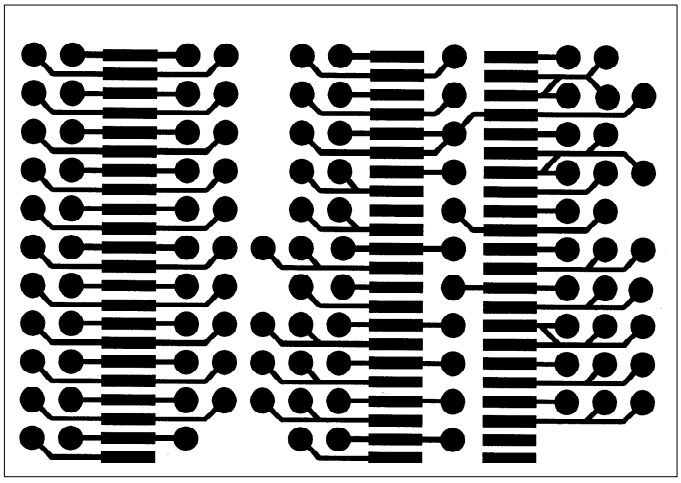


Fig. 2
Fan-Out Vias: Double-Sided Fine Pitch

It is this combination of features that provides the quantum leap in routability available with laser blind via technology. Designers utilizing laser blind via technology can place SMD components at minimum assembly parameters on both sides of a board and have confidence that the board can be interconnected. Blind via pads sizes should be increased by 0.13mm because of compound registration issues, on pads typically of 0.51mm which are drilling in volume production in multiple high stacks with vias diameters of 0.33mm and 0.25mm [4]

Once Blind vias rea incorporated into a design they are there for good. Also designers will continue to use them in upcoming design, even when their value may be considered minimal. [5] Adding two extra layers to a multilayer board will add a 15 and 20% cost penalty. [5]

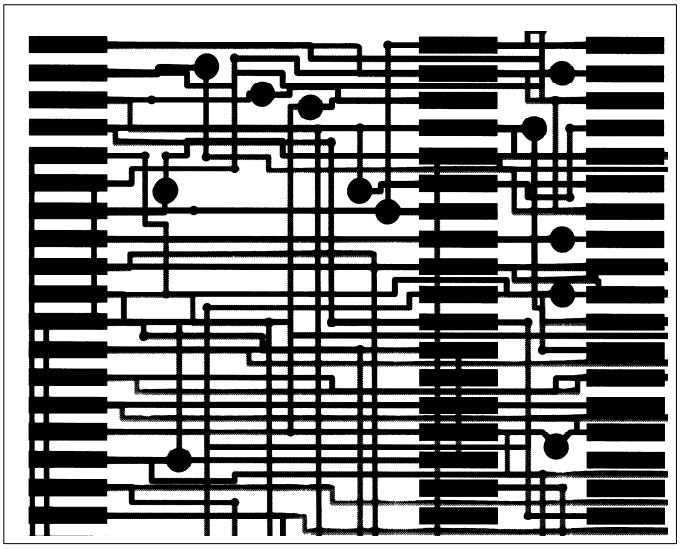


FIG. 3
Circuitry Easily Redesigned Using Blind Vias

Design Rules:

The first step, like in all circuit board fabrication, is to bring the CAD design into CAM tooling. The CAD design will have to have a pad stackup that defines the "windows" or etched openings necessary to allow the laser to remove the dielectric material.

The following drawings show the design rules for a QFP and BGA through final plating and etching:

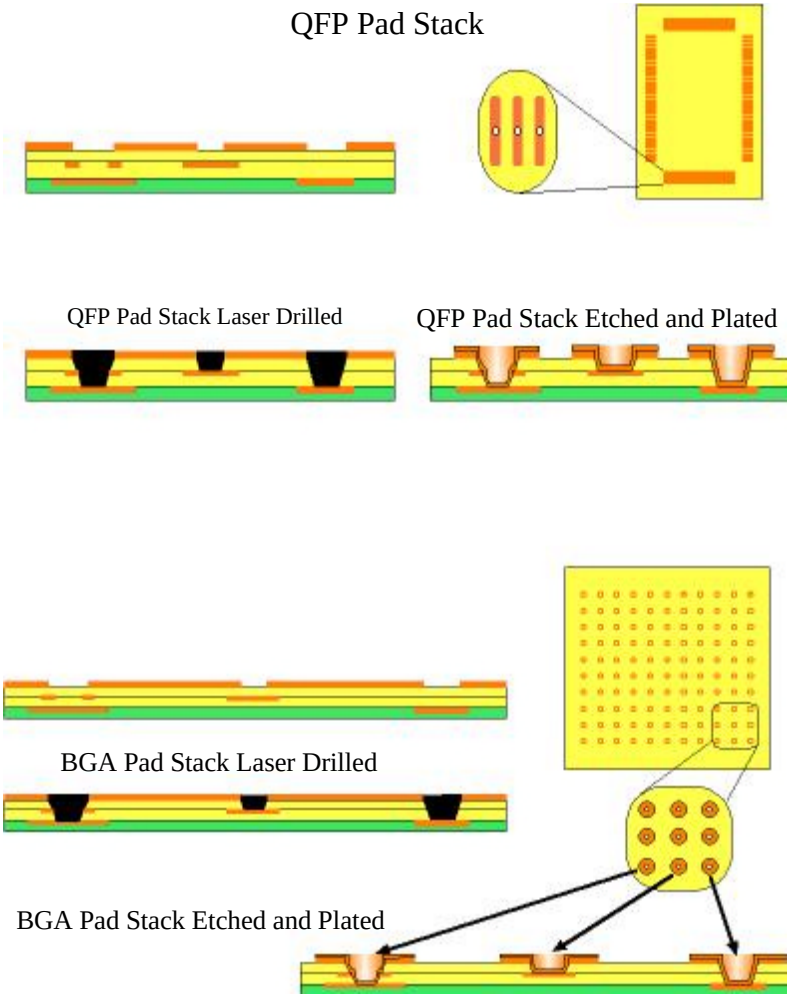


Fig. 4
Design Rules

Most circuit board wet processing lines can plate a 1:1 ratio (diameter to depth) blind via. Since gas entrapment can inhibit blind via plating in the electroless line, a “bump or thump” of the agitation racking system can readily release gas entrapped bubbles from the blind vias assuring continuous plating.

Polyimide (flex materials)
- PTFE (various Teflon® materials)

There are very little limitations to the diameter of laser drilled blind vias as fabrication processes mature (etching, plating etc.), narrow deep blind via interconnects will emerge to levels as deep as four layers down.

Material Layup:
Two lamination methods can be used to produce the multi-depth laser drilled blind vias:

1. Foil lamination: prepreg is used as the dielectric for the outer layer with copper foil. "Donuts" are etched in the layer two of the thin core material.

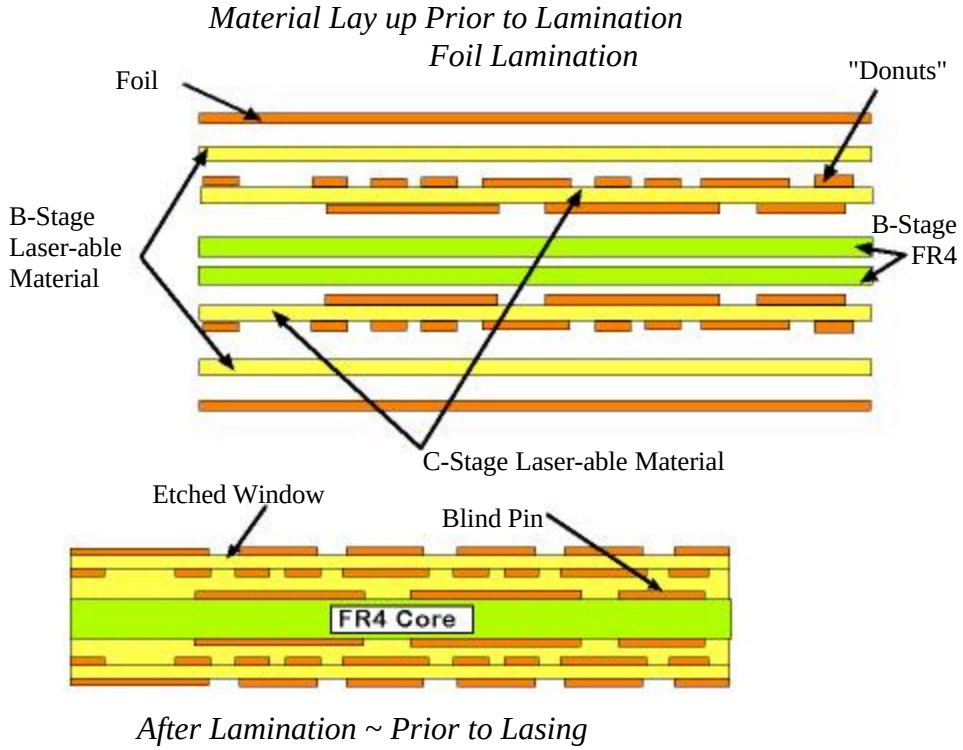


Fig. 6
Material Layup for Foil Lamination

2. Foil Cap Lamination: a thin core is used for the outer layer with a laser-able prepreg between circuit layers two and three.

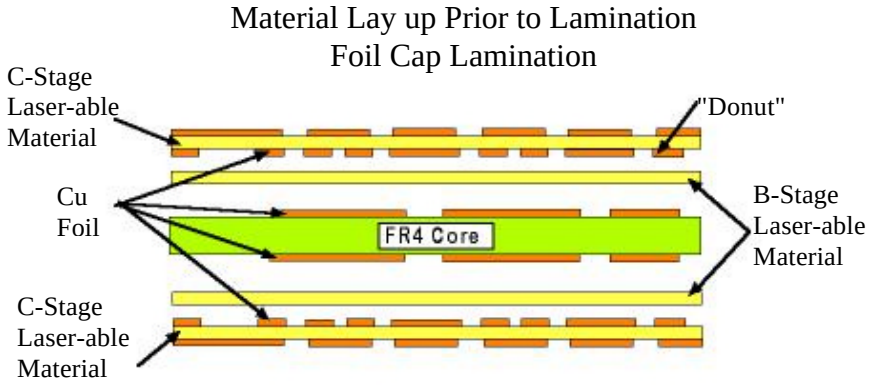


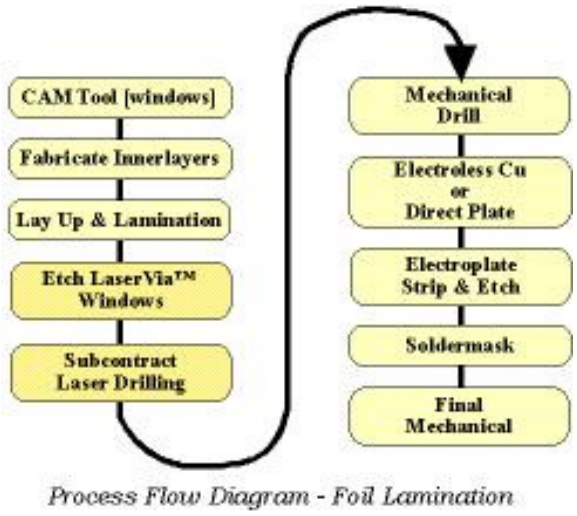
Fig. 7

Material Lay up for Foil Cap Lamination

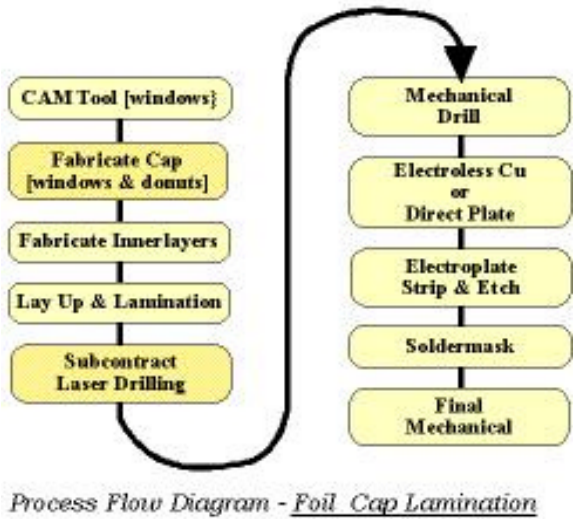
The preferred lamination process for multi-depth laser drilled blind vias fabrication is Foil Cap Lamination since the alignment of the outer windows and layer two "donuts" are imaged and etched at the same time. Using a typical inner layer registration technique for etching the outer windows and inner layer "donuts" relieves the problems that characteristically occur with material movement and "blind" registration to the layer two

Process Flow:

The two diagrams below depict typical laser blind via process flows, showing that laser drilling can be easily sequence subcontracted to a qualified laser drill source:



Process Flow Diagram - Foil Lamination



Process Flow Diagram - Foil Cap Lamination

Fig. 8
Process Flow for Foil Lamination and Foil Cap Lamination

Either foil lamination or foil cap lamination techniques can be used to produce multidepth blind vias. The choice is up to the fabrication process engineer and should be based on economics and the capability of the fabrication process. Inner layer registration of the blind pins or laser terminating pads is the most difficult and critical of the process steps.

CONCLUSION

Electronic components are demanding advances in circuit board packages to support higher density interconnections but at lower costs. Blind vias within surface mount pads are the best and quickest solution to this demand.

CAD tools are now capable of autorouting blind vias within surface mount pad to buried pins as the most effective interconnection on the circuit board. With the advantage of these Via-in-Pad interconnections the utilization of blind vias becomes a necessary connections technique. Blind vias, once a high cost, last resort option, are now becoming a widely available and economically advantageous alternative. Laser blind vias will become a widely used tool by designers meeting the high density board layout challenges of today.

The fabrication of blind vias within surface mount pad ("where they belong") can be processed in a number of fashions including: mechanical drilling, photovia, plasma etched and laser drilled. The two brightest blind via technologies situated for the leadership position are Photovia and Laser Drilling. Laser drilling is eminent as it can naturally and cost-effectively produce multi-depth blind via interconnections that can easily be introduced into today's circuit board fabrication process flow. Furthermore, work is progressing rapidly on Laser Drilling equipment that will shortly exceed the volume of panel output equivalency for multi-headed CNC mechanical drilling machines. [6,8]

BIOGRAPHIES

Larry Burgess has over thirty years experience in the interconnect packaging disciplines. He received a Bachelor's Degree in Chemistry from Lewis and Clark College. He managed the circuit board development laboratories at Tektronix prior to founding a start up called Interconnect Technology Inc., which introduced design, fabrication and surface mount assembly as a complete turnkey PCB facility in 1986. Interconnect Technology also introduced a laser drilled blind via technology as one of the first to place blind vias within surface mount pads. In 1995 Sandia National Laboratories purchased a LaserVia™ Technology R&D License from MicroPak Laboratories where he is Chief Technology Officer. He has consulted to several fortune 500 electronic manufactures and circuit board fabricators. Currently Mr. Burgess is rasing funds to open the first of several, sequence subcontract, circuit board laser drilling centers in the United States. Mr. Burgess has given multiple papers at Nepcon, IEPS, IPC and ISHM and written and contributed to multiple published articles. He is a member of IPC, IEPS, ISHM, SAMPE, SMTA and IEEE.

Paul Madden has over twenty-five years experience in the printed circuit board design And electronics packaging industry. At Loyola Marymount University Paul's major Course of study was Psychology. In ten years at Tektronix Inc., he worked as a PCB Designer, PCB Design Group Manager, and CAD Development Group Manager. In 1985 Paul became a cofounder and Design Group Manager at Interconnect Technology Inc., where he developed techniques to optimize the use of laser blind And buried vias in high density PCB's. In 1989 Paul became a partner and Design Group Manager at PCB West, a printed circuit board design service bureau, where he Remained until PCB West merged with Praegitzer Industries in March of this year. Currently, Paul is a Design Group Supervisor at Praegitzer Design in Hillsboro Oregon.

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